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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/695,969 | 10/29/2003 | Hiroaki Ohkubo | NECF 20.702 | 7995 |

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KATTEN MUCHIN ROSENMAN LLP
575 MADISON AVENUE
NEW YORK, NY 10022-2585

| EXAMINER | |
|---|---|
| MOVVA, AMAR | |

| ART UNIT | PAPER NUMBER |
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| 2894 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/695,969 | OHKUBO ET AL. | |
| | Examiner | Art Unit | |
| | AMAR MOVVA | 2894 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,5 and 11-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 11-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1-27-09, 10-15-08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102/103*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,5,11-13, 16, and 18 rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Williams '989.

a. Williams discloses a semiconductor integrated circuit, comprising: a silicon substrate (111, fig. 25p) having a substantially planar top surface; a silicon epitaxial layer (121,121e, fig. 25p) having a lower resistivity than the resistivity of said silicon substrate (col. 10, lines 50-55) the epitaxial layer having a substantially planar lower epitaxial surface, the epitaxial layer being formed upon the top substrate surface so that the lower epitaxial surface and the top substrate surface are adjacent; a first and second circuit section formed in said silicon epitaxial layer (both sides of ISO layer) each circuit section spaced apart from the top substrate surface by a respective portion of the silicon epitaxial laver; and a device isolation region (129a,125, fig. 25p) formed toward an inner part of the

epitaxial layer from the top surface of the epitaxial layer between said first and second circuit sections. A digital circuit is formed on said first circuit section, and an analog circuit is formed on said second circuit section (circuit can be used in such a fashion). The silicon epitaxial layer is a single layer (fig. 25p). The silicon epitaxial layer is a p-type bulk epitaxial layer (fig. 25p). The silicon substrate comprises a p-type bulk substrate (fig. 25p). The p-type bulk epitaxial layer is formed by a chemical vapor deposition method (see below). The silicon epitaxial layer has a thickness of 5 micrometers (since the ISO regions are graded 129a/125 allow for a thickness of 121/121e of up to 20 microns (col. 13, lines 40-60)) and a resistivity of 10 Ohm—cm (col. 13, lines 40-60). Said silicon substrate and said silicon epitaxial layer are of the same conductivity type (fig. 25p). Additionally Williams discloses in the embodiments (especially of fig. 22) wherein the n+ buried layer 123 and 125 maybe optionally deleted (lines 4-10, col. 12).

b. However, assuming *arguendo* that the reference must be so narrowly interpreted so as to mean that Williams fig. 25p does not disclose that that n+ buried layer 123 and 125 may be optionally deleted the claims would not be anticipated. Nonetheless, it would have been obvious to one of ordinary skill in the art the time of the invention to have eliminated at least the n+ buried layer (123, fig. 25p) in Williams in order to reduce fabrication cost/complexity by eliminating the need to form additional diffusion layer(s).

4. Claims 1,12, and 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Cricchi '349. Cricchi discloses a semiconductor integrated circuit, comprising: a silicon substrate (12,14 fig. 1); a silicon epitaxial layer (24,32 fig. 1) that and has a lower resistivity than the resistivity of said silicon substrate (col. 3); first and second circuit sections formed in said silicon epitaxial layer (both sides of FOX layers); and a device isolation region (46, fig. 1) projecting from said silicon substrate up to a surface of each of said first and second circuit sections between said first and second circuit sections (fig. 1). The portions of the epitaxial layer under both the first and second circuits are in contact with the substrate (fig. 1). Said silicon epitaxial layer is a p-type bulk epitaxial layer (32, fig. 1). Said silicon substrate comprises a p-type bulk substrate (14, fig. 1).

PLEASE NOTE: The recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See, e.g., *In re Pearson*, 18 1 USPQ 641 (CCPA); *In re Minks*, 169 USPQ 120 (Bd Appeals); *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 136 USPQ 458, 459 (CCPA 1963); See MPEP §2114. The recitation of the use of individual circuit sections in an analog/digital fashion, does not distinguish the present invention over Williams 989 who teaches the structure as claimed.

PLEASE NOTE: Claim 16 contains process limitations regarding the use of CVD. These limitations invoke the Product-by-Process doctrine. Product-by-process limitations are not limited by the manipulations of the recited steps, only the structure implied by the steps (MPEP 2113). Specifically the use of CVD p-epitaxial layer does not appear to structurally distinguish the invention over the resulting structure produced by the prior art. The burden to show that the claimed method necessarily distinguishes over the prior art is on the applicant.

***Claim Rejections - 35 USC § 103***

5. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams '989 in view of Cricchi '349.

c. Williams discloses the device of claims 1 and 13 but does not expressly disclose that the silicon substrate is between 100 times the restivitity than the silicon epitaxial layer.

d. Cricchi discloses a semiconductor integrated circuit wherein a silicon substrate has a restivity of 1000 Ohm-cm (col. 3).

e. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Williams 10-60 Ohm-cm silicon substrate to a 1000 Ohm-cm substrate in order to reduce interference from other parts of the IC as well as effective reduction in losses generated by the passive elements (col. 3 of Cricchi).

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cricchi '349.

a. Cricchi discloses the device of claim 13 and further that the silicon substrate has a restivity of 1000 Ohm-cm (col. 3) but does not expressly disclose that the thickness of the substrate is 0.7 mm.

b. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have made Cricchi's substrate thickness 0.7mm , since it has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 in order to ensure sufficient thickness to reduce interference from other parts of the IC as well as effective reduction in losses generated by the passive elements.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams '989 in view of Cricchi '349.

a. Williams discloses the device of claim 13 but does not expressly disclose that the silicon substrate has one hundredth less of an impurity concentration than the silicon epitaxial layer.

b. Nevertheless it would have been obvious to one of ordinary skill in the art at the time the invention was made to have had the silicon substrate one hundredth less of an impurity concentration than the silicon epitaxial layer since it has been held that where the general conditions of a claim are disclosed in prior

art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. in order to reduce interference from other parts of the IC.

***Response to Arguments***

Applicant's arguments filed 10-21-08 have been fully considered but they are not persuasive.

a. As a preliminary matter, examiner notes that arguments toward that the instant device is less complex to produce, cheaper, and produces less noise than the prior art is not sufficient to traverse the rejection. To the contrary only the structural limitations of the claim need be met by the prior art.

b. Applicant argues that Williams does not disclose a lower surface of the epitaxial layer and the upper surface of the substrate to be adjacent because of a n+ buried layer. This is inaccurate, examiner uses a 102/103 rejection to meet this limitation. Williams discloses alternative embodiments where the n+ buried layer is eliminated. In the context of the Williams reference this would allow the instant n+ buried layer to be optional. Furthermore even assuming arguendo that such a feature is not an option, Williams would be motivated by the alternative embodiment to eliminate the n+ buried layer in order to reduce fabrication cost/complexity by eliminating the need to form additional diffusion layer(s). Examiner notes that the 103 portion is over different embodiments of the same reference.

c. Applicant's remaining arguments have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AMAR MOVVA whose telephone number is (571)272-9009. The examiner can normally be reached on 7:30 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amar Movva
Examiner
Art Unit 2894

am

/Bradley K Smith/
Primary Examiner, Art Unit 2894